5W Wireless Power Receiver with Charger

1 Features

- **High-integration wireless power receiving SOC**
  - ✧ Built-in 32-bit MCU
  - ✧ Built-in 10k bytes MTP, 1k bytes RAM
  - ✧ Built-in multi-channel 12bit SAR ADC
- **Support 5W wireless power reception**
  - ✧ Built-in high-efficiency full-bridge synchronous rectifier circuit
  - ✧ Built-in wireless charging overvoltage protection circuit
  - ✧ Built-in ASK modulation circuit
  - ✧ Built-in FSK demodulation circuit, support private protocol
  - ✧ Support the latest protocol standard of WPC Qi
- **Built-in voltage regulator LDO**
  - ✧ Output voltage gear 3.0~ 5.5V programmable
  - ✧ Output current up to 1.6A
  - ✧ Undervoltage protection, overcurrent protection
- **Anti-offset ability**
  - ✧ LDO Input Dynamic Power Management (DPM)
  - ✧ LDO output current dynamic limit (Current Limit)
- **Built-in 800mA Linear Charger**
- **Multiple power supply methods**
  - ✧ Wireless power supply, VRECT pin input
  - ✧ Wired power supply, VBUS pin input
  - ✧ Battery power supply, VBAT pin input
  - ✧ Support wired charging and wireless charging path switching
- **Reliable over temperature, over voltage and over current protection circuit**
- **Power consumption is less than 2uA in deep sleep mode**
- **4mm*4mm 0.4 pith QFN28 package**

2 Applications

- Wireless power receiving device
- Wireless charging mobile juicing cup
- Wireless charging mobile fruit and vegetable washing machine
- Wireless charging electric toothbrush

3 Description

IP6833 is a highly integrated wireless charging receiver SOC that supports the WPC Qi standard. The chip integrates a high-efficiency full-bridge synchronous rectification circuit to realize AC-DC conversion. The rectified output voltage, VRECT, is regulated by the internal LDO and outputs a stable DC voltage for subsequent loads.

IP6833 built-in linear charging module provides a maximum charging current of 800mA.

IP6833 built-in 32-bit MCU and rich peripheral resources, so external MCU can be omitted during product development. IP6833 integrates wireless reception + lithium battery line charging + MCU into one. Its deep sleep mode with 2uA power consumption is more suitable for product development with batteries.

IP6833 uses QFN28 (4mm*4mm) package, with peripheral streamlined application circuit, which greatly saves PCB footprint and can be easily integrated into products with compact space.

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4 Reversion History

Note: Page numbers of previous editions may differ from those of the current edition.

Version V1.0 changed in February 2023	Page
• First Release	1

5 Application Diagram

5.1 Wireless Power Receiving Application

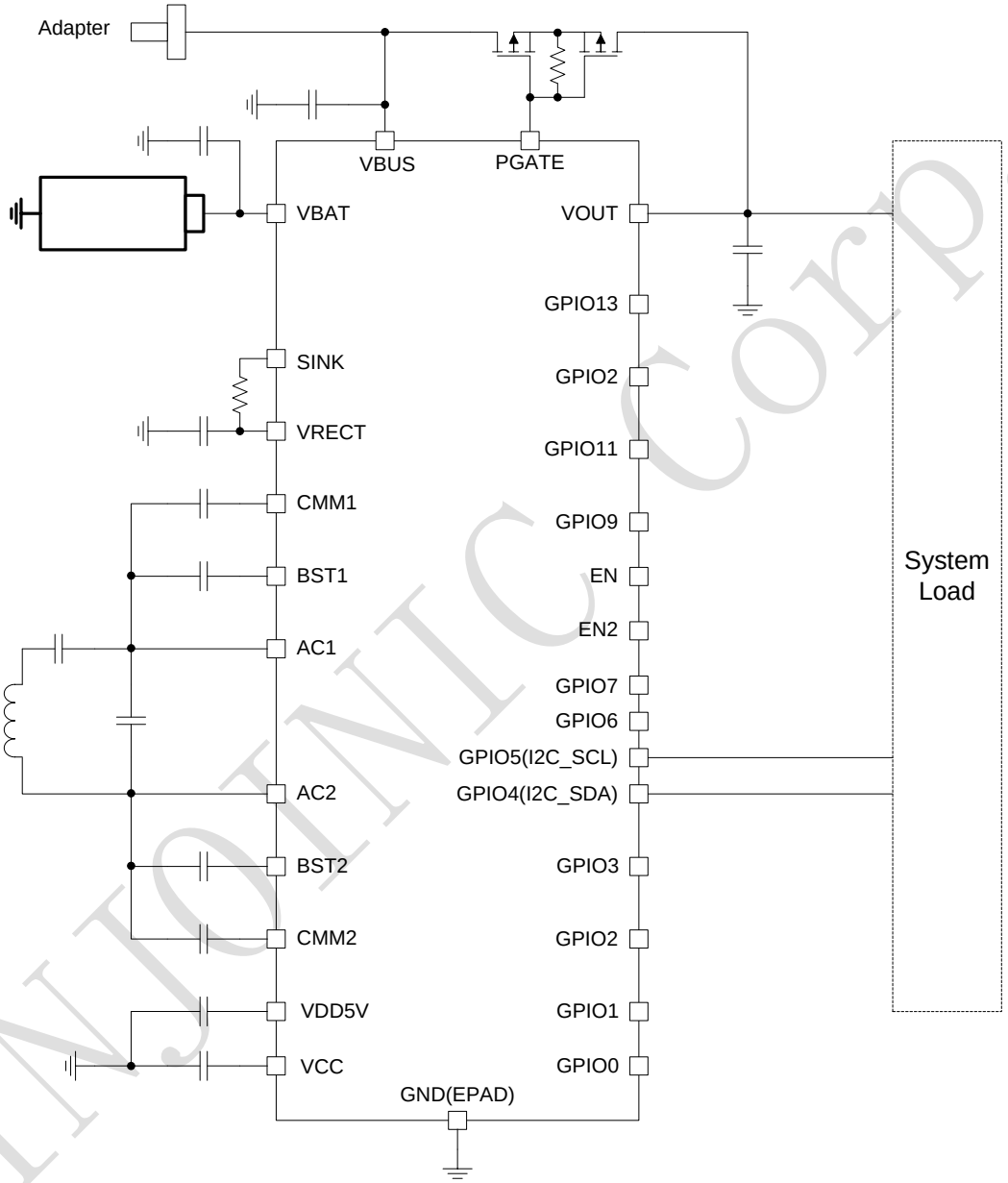


Figure 1 IP6833 Wireless Power Receiving Application

5.2 Electric Toothbrush SOC Application

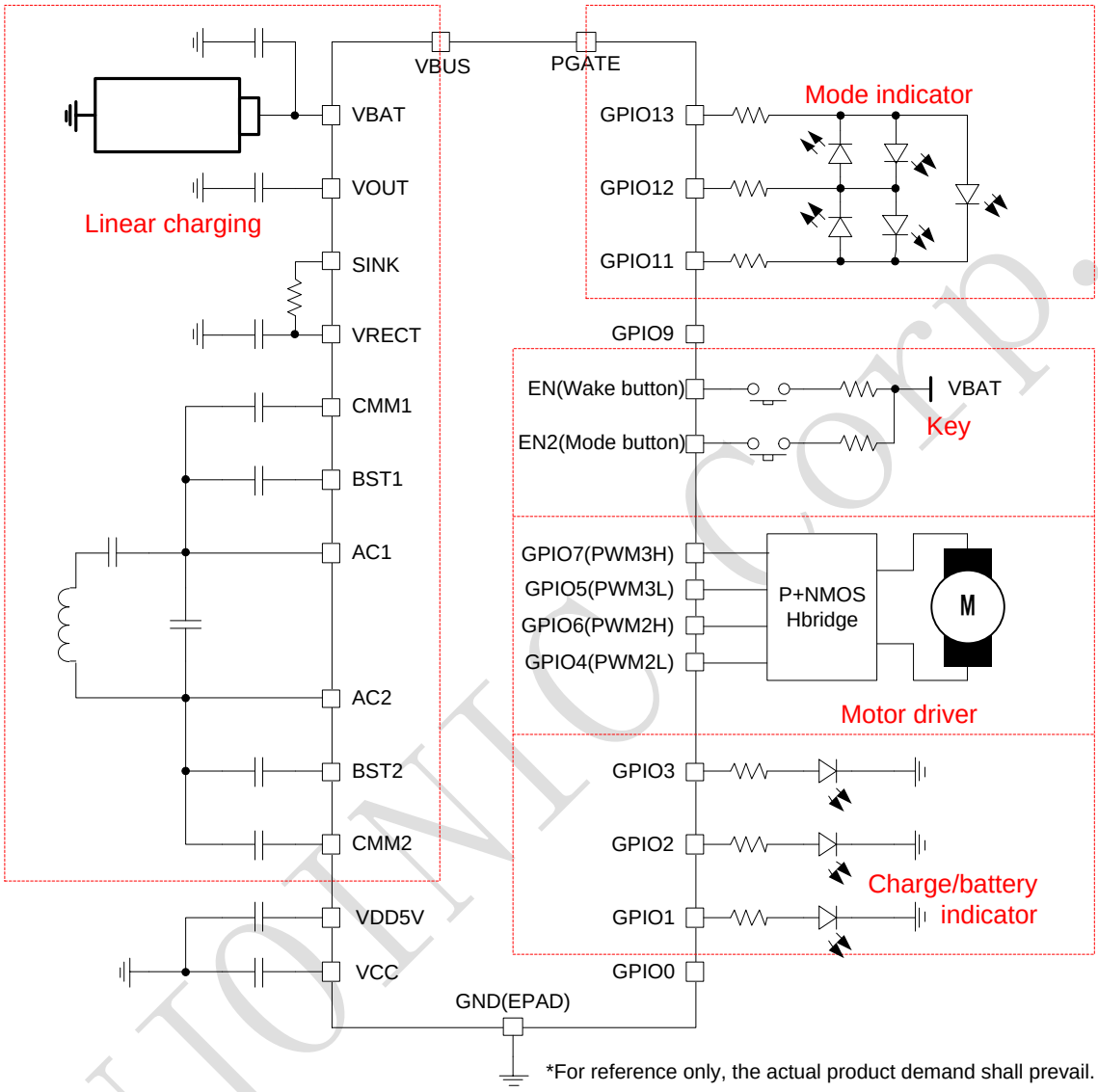


Figure 2 IP6833 Single Chip Electric Toothbrush Application

6 Pin Definition

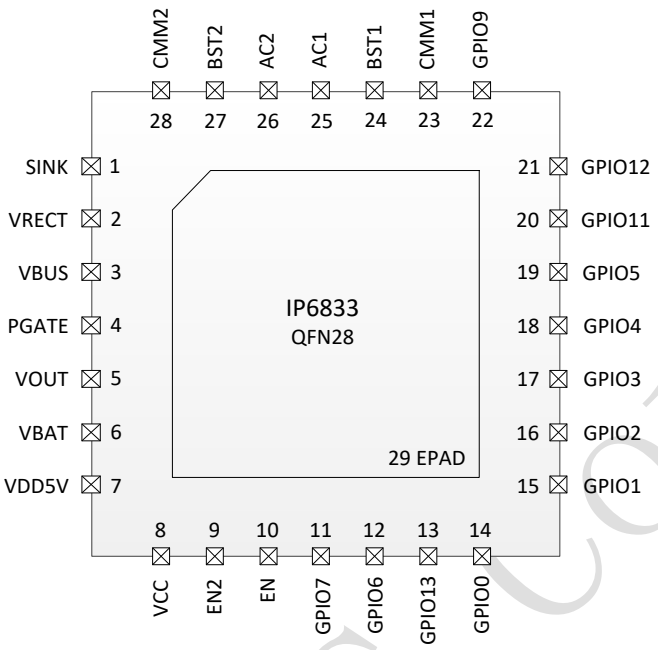


Figure 3 IP6833 Pin Definition

Pin Num	Name	I/O	Description
1	SINK	I	VRECT voltage clamping port.
2	VRECT	O	Synchronous rectification output filter port.
3	VBUS	I	Wired charging input port.
4	PGATE	O	Wired charging and wireless charging path switching driver output.
5	VOUT	O	Power LDO output port.
6	VBAT	I/O	Battery port, connected to battery positive pole.
7	VDD5V	O	5V power supply, connect to PGND with 2.2uF capacitor.
8	VCC	O	3.3V power supply, connect to PGND with 2.2uF capacitor.
9	EN2	I	Enable port, effective at high level.
10	EN	I	Enable port, effective at high level.
11	GPIO7	O	GPIO
12	GPIO6	O	GPIO
13	GPIO13	O	GPIO
14	GPIO0	O	GPIO
15	GPIO1	O	GPIO
16	GPIO2	O	GPIO
17	GPIO3	O	GPIO
18	GPIO4	O	GPIO
19	GPIO5	O	GPIO
20	GPIO11	O	GPIO
21	GPIO12	O	GPIO
22	GPIO9	O	GPIO
23	CMM1	O	ASK modulation port, connect to AC1 with 10~22nF capacitor.
24	BST1	O	Bootstrap capacitors for driving the high side FETs of the synchronous rectifier. Connect to AC1 with 22nF capacitor.
25	AC1	I	AC input from receiver coil.
26	AC2	I	AC input from receiver coil.
27	BST2	O	Bootstrap capacitors for driving the high side FETs of the synchronous rectifier. Connect to AC2 with 22nF capacitor.
28	CMM2	O	ASK modulation port, connect to AC2 with 10~22nF capacitor.
29	PGND	-	System and power ground.

7 System Diagram

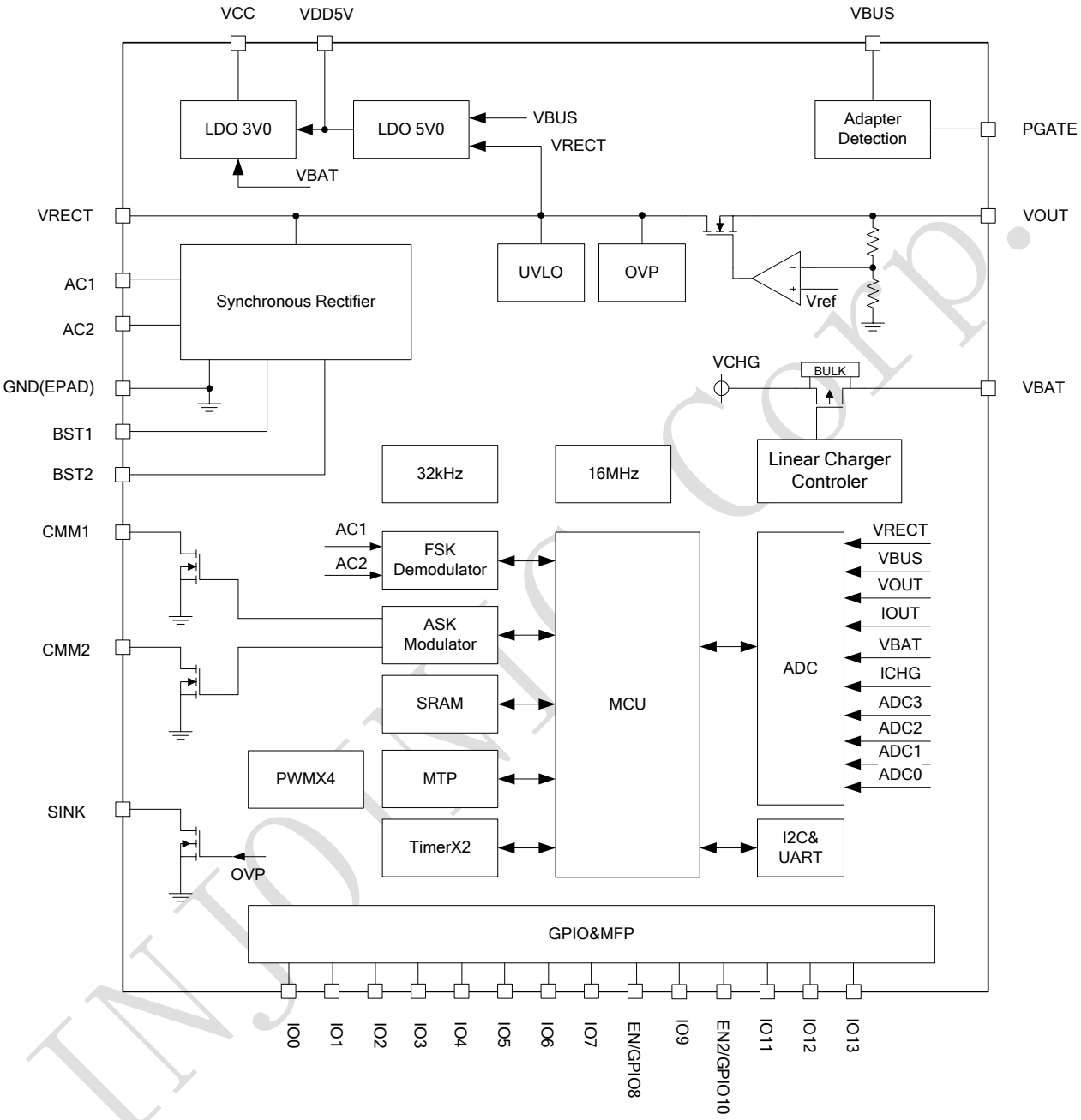


Figure 4 IP6833 Internal System Diagram

8 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Input Voltage Range	AC1/2	-0.3	20	V
	VBUS	-0.3	20	V
	VBAT	-0.3	8	V
	SINK	-0.3	20	V
Output Voltage Range	VRECT	-0.3	20	V
	VOUT	-0.3	8	V
	VDD5V/VCC	-0.3	8	V
	PGATE	-0.3	20	V
	CMM1/2	-0.3	20	V
	BST1/2	-0.3	30	V
I/O Voltage Range	GPIO0-13,EN,EN2	-0.3	8	V
Storage Temperature Range	T_{stg}	-55	150	℃
Thermal Resistance (Junction to Ambient)	θ_{JA}	40		℃/W
ESD (Human Body Model)	ESD	4		KV

*Stresses beyond these listed parameter may cause permanent damage to the device.

Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

9 Recommended Operating Conditions

Parameter	Symbol	Min	Type	Max	Unit
Rectified Output Voltage	VRECT	3	5	14	V
Load Current	I	0	1	1.5	A
VBUS Input Voltage	VBUS	4.5	-	12	V
Operating Temperature	T_A	0	-	85	℃

*Device performance cannot be guaranteed when working beyond these Recommended Operating Conditions.

10 Electrical Characteristics

Unless otherwise specified.T_A=0°C ~85°C

Parameter	Symbol	Test conditions	Min	Type	Max	Unit
VRECT						
V_{RECT}_UVLO Threshold	V_{RECT_UVLO}	V_{RECT}:5V->0V	2.8	2.9	3.0	V
V_{RECT}_UVLO Threshold Hysteresis	V_{RECT_UVLO} Hyteresis	V_{RECT}: V_{RECT_UVLO} ->5V		0.25		V
V_{RECT} OVP Threshold	V_{RECT_OVP}	V_{RECT}:5V->20V	14.5 16.5	15 17	15.5 17.5	V
V_{RECT} OVP Recover Threshold	V_{RECT_OVP} Recover	V_{RECT}: V_{RECT_OVP} ->5V		12		V
VBUS						
V_{BUS} Input Voltage	V_{BUS}		4.5	5	6	V
V_{BUS}_UVLO Threshold	V_{BUS_UVLO}	V_{BUS}:5V->0V	3.8	3.9	4.0	V
V_{BUS}_UVLO Threshold Hysteresis	V_{BUS_UVLO} Hyteresis	V_{BUS}: V_{BUS_UVLO} ->5V		0.3		V
V_{BUS}_OVP Threshold	V_{BUS_OVP}	V_{BUS}:5V->9V		6.5		V
V_{BUS}_OVP Threshold Hysteresis	V_{BUS_OVP} Hyteresis	V_{BUS}: V_{BUS_OVP} ->5V		0.5		V
LDO						
LDO Output Voltage	V_{SET_LDO}	V_{RECT} > Vout_ldo	3.0V~5.5V Programmable			V
LDO Voltage Regulation Step	V_{STEP_LDO}		50			mV
LDO Input Dynamic Power Management	V_{DPM_LDO}		3.9V~4.6V Programmable			V
LDO Output Current Limit	I_{LIMIT_LDO}	Programmable			1600	mA
Quiescent Current						
V_{RECT} Quiescent Current	I_{Q_VRECT}	V_{RECT}=5V,LDO is off		2	5	mA
V_{BUS} Quiescent Current	I_{Q_VBUS}	V_{BUS}=5V only		2	5	mA
Sleep Mode Current	$I_{DeepSleep}$	V_{BAT}=3.7V only,IC deep sleep			2	uA
Charger						
CV Constant Voltage Charging Voltage	$CV_{4.2V}$	Programmable	4.15	4.20	4.24	V
	$CV_{4.3V}$		4.28	4.30	4.34	V
	$CV_{4.35V}$		4.33	4.35	4.4	V

	$CV_{4.4V}$		4.38	4.40	4.44	V
Charge Stop Current	$I_{VIN\ stop}$	Programmable		50	100	mA
Linear Charging Current	I_{chg}	Programmable			800	mA
Trickle Charging Current	I_{TRKL}	Programmable		0.1*CC		
Trickle Charge Stop Voltage Threshold	V_{TRKL}		2.9	3	3.1	V
Recharge Voltage Threshold	V_{RCH}		4.07	4.1	4.13	V
System						
VDD5V	VDD5V	1uF, I_{VDD5V} =30mA	4.5	5	5.5	V
VCC	VCC	V_{BAT}=3.7V		3.1		V
VCC Load Capacity	I_{VCC}	VCC Maximum load current			50	mA
GPIO Logic High Level	V_{IH}	GPIO0~5,GPIO9, GPIO11~13		0.7*VCC		V
GPIO Logic Low Level	V_{IL}	GPIO0~5,GPIO9, GPIO11~13		0.3*VCC		V
EN/EN2 Wake-up Level	V_{EN_WAKE}		1.5			V
Thermal Shut Down Temperature	T_{OTP}	Rising temperature	130	140	150	℃
Thermal Shut Down Hysteresis	ΔT_{OTP}		30	40	50	℃

11 Function Description

11.1 Synchronous Rectification

IP6833 integrates a high-efficiency full-bridge synchronous rectification module, which consists of a logic detection circuit, four N-MOSFETs and a driver circuit. Initially, AC current from the receiving coil flows through the parasitic diodes of the MOSFET, providing the chip with a start-up voltage. When the chip is powered on, the system switches the working mode of the rectifier bridge according to the load current. The rectifier bridge works in asynchronous mode (parasitic diode mode) at light load, and synchronous mode (MOSFET switch mode) at heavy load. The switching of working mode ensures high efficiency and stability of wireless charging.

11.2 Wireless Power Supply

IP6833 integrates wireless charging ASK modulation circuit and FSK demodulation circuit to realize two-way wireless charging communication and support private protocol development.

IP6833 integrates rectifier overvoltage protection circuit, when the rectifier voltage VRECT exceeds 15V (the gear can be configured by software), it will trigger the VRECT voltage clamping function to limit the VRECT voltage.

11.3 Wired Power Supply

IP6833 supports VRECT (wireless), VBUS (wired) and VBAT (battery) for power supply, and supports path switching between wired power supply and wireless charging.

11.4 Voltage Regulated LDO

Due to the position freedom of wireless charging, the rectifier voltage VRECT is not a stable voltage, and the rectifier voltage VRECT fluctuates greatly during the process of moving the charging equipment. IP6833 integrates a regulated LDO. The rectified voltage, VRECT, passes through the internal regulated LDO to provide a stable DC voltage to the downstream load. The output voltage and current of the regulated LDO can be set by software, and the voltage can be set in the range of 3.0V~5.5V in steps of 50mV; The output current limit setting range is 0~1600mA in steps of 50mA.

The regulated LDO has safety protection functions such as input undervoltage protection, input dynamic power management (DPM), output overcurrent protection, and output current limiting. When the charging device moves or deflects, the rectifier voltage VRECT will drop. When it falls below the DPM threshold of LDO, the regulated LDO will automatically reduce the output current, maintain the uninterrupted wireless charging, and improve the anti-deflection ability of wireless charging.

11.5 Linear Charging

IP6833 integrates an 800mA linear lithium battery charging module. The charging current and voltage range can be set by software.

IP6833 supports the charging voltage dynamic tracking function, dynamically adjusts the voltage difference between the rectifier output VRECT and the battery end according to the charging current,

improves the system efficiency and reduces the temperature rise.

11.6 Low Power Mode and Wake Up

IP6833 supports deep sleep mode, and the power consumption in deep sleep mode is less than 2uA. In deep sleep mode, the IP6833 can be woken up by pulling the EN or EN2 pin high by 50ms.

11.7 MCU

IP6833 integrates 32-bit MCU, and has rich peripheral resources such as Timer, PWM, ADC, I2C, UART, GPIO, etc., which is convenient for the customization of the whole product function without the need for external MCU.

12 Typical Application Schematic

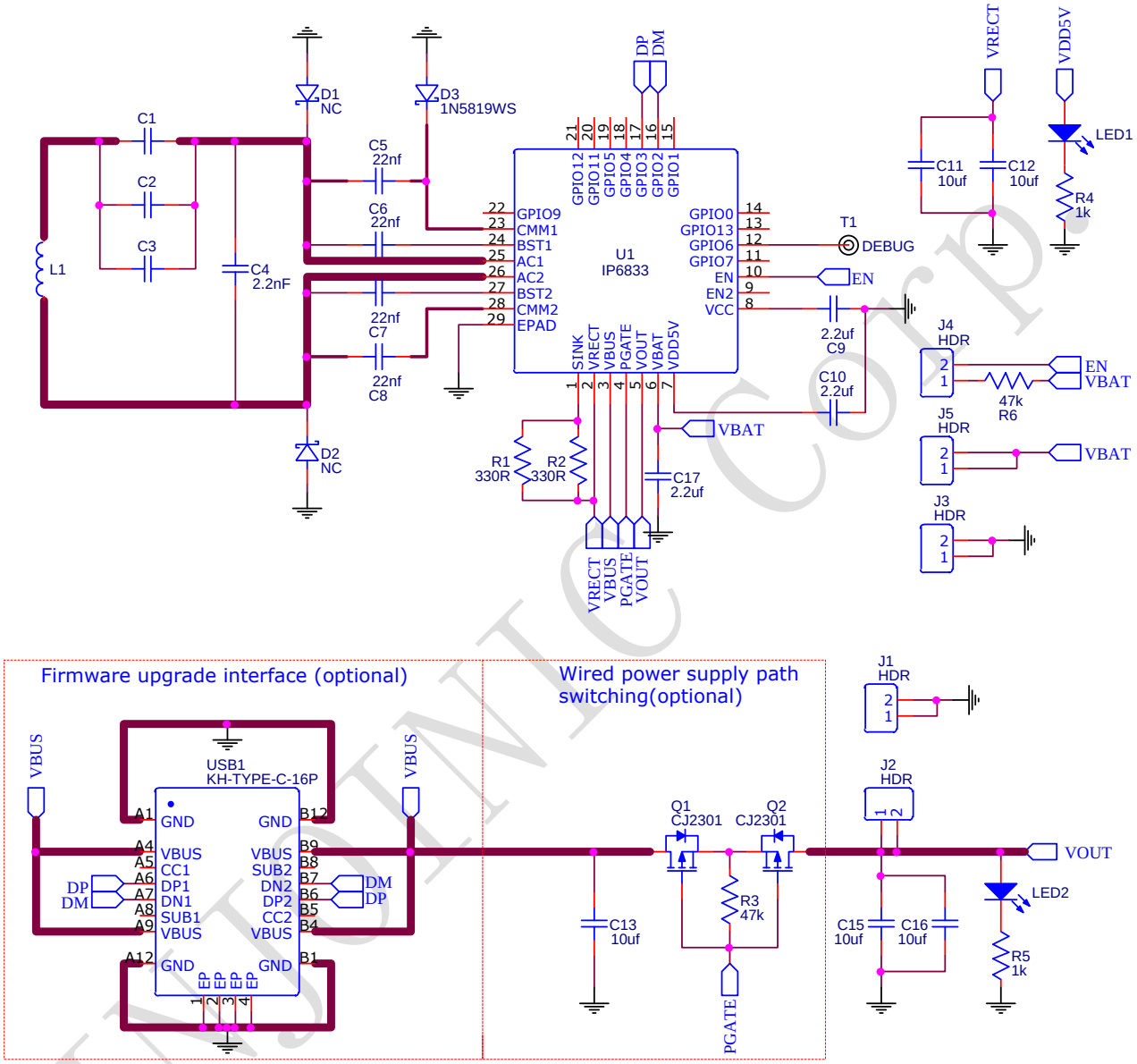
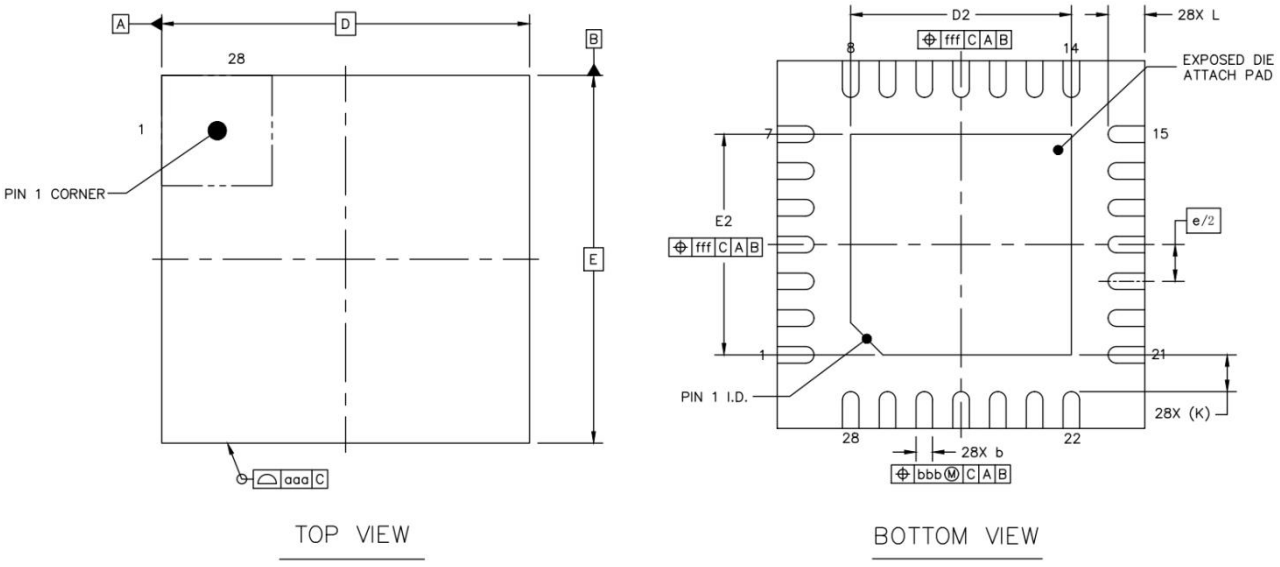


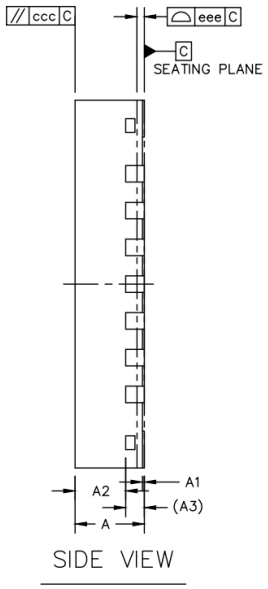
Figure 5 IP6833 Typical Application Schematic

13 BOM

Num	Part Name	Position	Specification	Quantity
1	Resonant Capacitor	C1,C2,C3	C0603-10%-50V	3
2	Resonant Inductance	L1	Inductance parameters are selected according to the actual project	1
3	2.2nF	C4	C0603-10%-50V	1
4	22nf	C5,C6,C7,C8	C0603-10%-50V	4
5	2.2uf	C9,C10,C17	C0603-10%-16V	3
6	10uf	C11,C12,C13,C15,C16	C0603-10%-16V	5
7	NC	D1,D2	SOD-323_L1.6-W1.3-LS2.7-RD	2
8	1N5819WS	D3	SOD-323_L1.6-W1.3-LS2.7-RD	1
9	HDR	J1,J2,J3,J4,J5	HDR-M-2.54_1X2	5
10	LED	LED1,LED2	LED0603_RED	2
11	CJ2301	Q1,Q2	SOT-23-3	2
12	330R	R1,R2	R0805-5%-0.75W	2
13	47k	R3,R6	R0603-5%	2
14	1k	R4,R5	R0603-5%	2
15	TYPE-C-16P	USB1	USB-C-SMD_KH-TYPE-C-16P	1
16	IP6833	U1	QFN28-4mm*4mm	1

14 Package





UNIT : mm		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	2.3	2.4	2.5
	Y	E2	2.3	2.4	2.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

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