
Wireless Charging Transmitter Controller

1 Features

- **Supports the latest WPC standard**
- ◇ Support Qi protocol BPP, EPP, QI2.0 MPP certification
- **Working voltage**
- ◇ 4V ~ 20V
- **Support up to 30W applications**
- **Support 5~15W multiple applications**
- ◇ Power backwards compatible
- **Integrated H-bridge drive**
- **Integrated internal voltage & current demodulation**
- **Support FOD foreign object detection function**
- ◇ Static FOD detection
- ◇ Dynamic FOD detection
- **Support external passive crystal oscillator**
- **Support CBB/NPO capacitors**
- **Support Q value detection**
- **Dynamic Power Management (DPM) for USB power supply with insufficient power supply**
- **Input overvoltage, overcurrent, undervoltage, NTC overtemperature protection function**
- **Integrated 32KB MTP to support repeated firmware upgrades**
- **Support PD3.0, as well as a variety of DP&DM fast charging protocols**
- **Package 5 mm × 5 mm 0.5pitch QFN32**

2 Applications

Wireless charging base

3 Description

IP6802 is a wireless charging transmitter control SOC chip with internal integration of 32-bit MCU, ADC, Timer, I2C, H-bridge driver, ASK demodulation & decoding and rich IO resources, which can customize various Qi protocol wireless charging solutions and pass certification tests.

IP6802 integrates multiple charging head fast charging protocols, can automatically apply high voltage, and supports wireless charging fast charging protocols.

IP6802 integrates rich IO resources and supports customization of indicator effects, and users can also customize the indicator through the PC upper computer.

目录

1 Features.....	1
2 Applications	1
3 Description.....	1
4 Reversion History	3
5 Pin Configuration And Function.....	3
5.1 Pin Description	3
6 Functional Block Diagram	5
7 Absolute Maximum Ratings.....	6
8 Recommended Operating Conditions	6
9 Electrical Characteristics	6
10 Function Description.....	7
10.1 Fast Charge Input Request.....	7
10.2 Full Bridge Drive and Digital Demodulation	7
10.3 DPM	8
10.4 FOD Parameter Adjustment.....	8
10.5 NTC Thermal Protection	8
10.6 Charging Indicator.....	9
10.7 Efficiency Curve Test.....	9
11 Application Notes.....	11
12 Firmware Upgrade Instructions	11
13 Typical Application Schematic.....	12
14 Layout Notes	13
15 BOM.....	15
16 Package.....	16
17 Silk Information.....	17
18 IMPORTANT NOTICE	18

4 Reversion History

Note: The page number of the previous version may differ from the page number of the current version.

Changes from Revision V1.0 (April 2023) Page

- First Release 1

Changes from Revision V1.0 (September 2024) to Revision V1.10 Page

- Add MPP description 1
- Added MPP schematic..... 12

5 Pin Configuration And Function

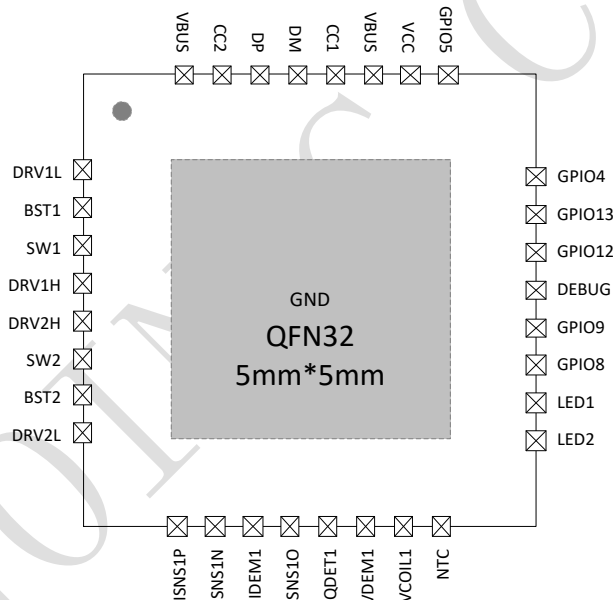


Figure 1 IP6802 Pin Diagram

5.1 Pin Description

Pin No.	Pin Name	Description
1	DRV1L	DRV1 low-side drive
2	BST1	DRV1 bootstraps, Series 47nF capacitors to SW1
3	SW1	DRV1 Half-bridge switch node
4	DRV1H	DRV1 high-side drive
5	DRV2H	DRV2 high-side drive
6	SW2	DRV2 Half-bridge switch node

7	BST2	DRV2 bootstraps, Series 47nF capacitors to SW2
8	DRV2L	DRV2 low-side drive
9	ISNS1P	VBUS current positive sense input
10	ISNS1N	VBUS current negative sense input
11	IDEM1	ASK demodulate inputs
12	ISNS1O	Sample current amplified output
13	QDET	Q-value detection input
14	VDEM1	ASK demodulate inputs
15	VCOIL1	Coil voltage input pin
16	NTC	NTC input pin
17	LED2	LED2 output
18	LED1	LED1 output
19	GPIO8	GPIO8
20	GPIO9	GPIO9
21	GPIO10	Debug Pin
22	GPIO12	GPIO12
23	GPIO13	GPIO13
24	GPIO4	GPIO4
25	GPIO5	GPIO5
26	VCC	Internal VCC supply, external 4.7uF capacitor to GND
27	VBUS	External input voltage
28	CC1	Type_C detect pin CC1
29	DM	USB DM
30	DP	USB DP
31	CC2	Type_C detect pin CC2
32	VBUS	External input voltage
33	GND	GND

6 Functional Block Diagram

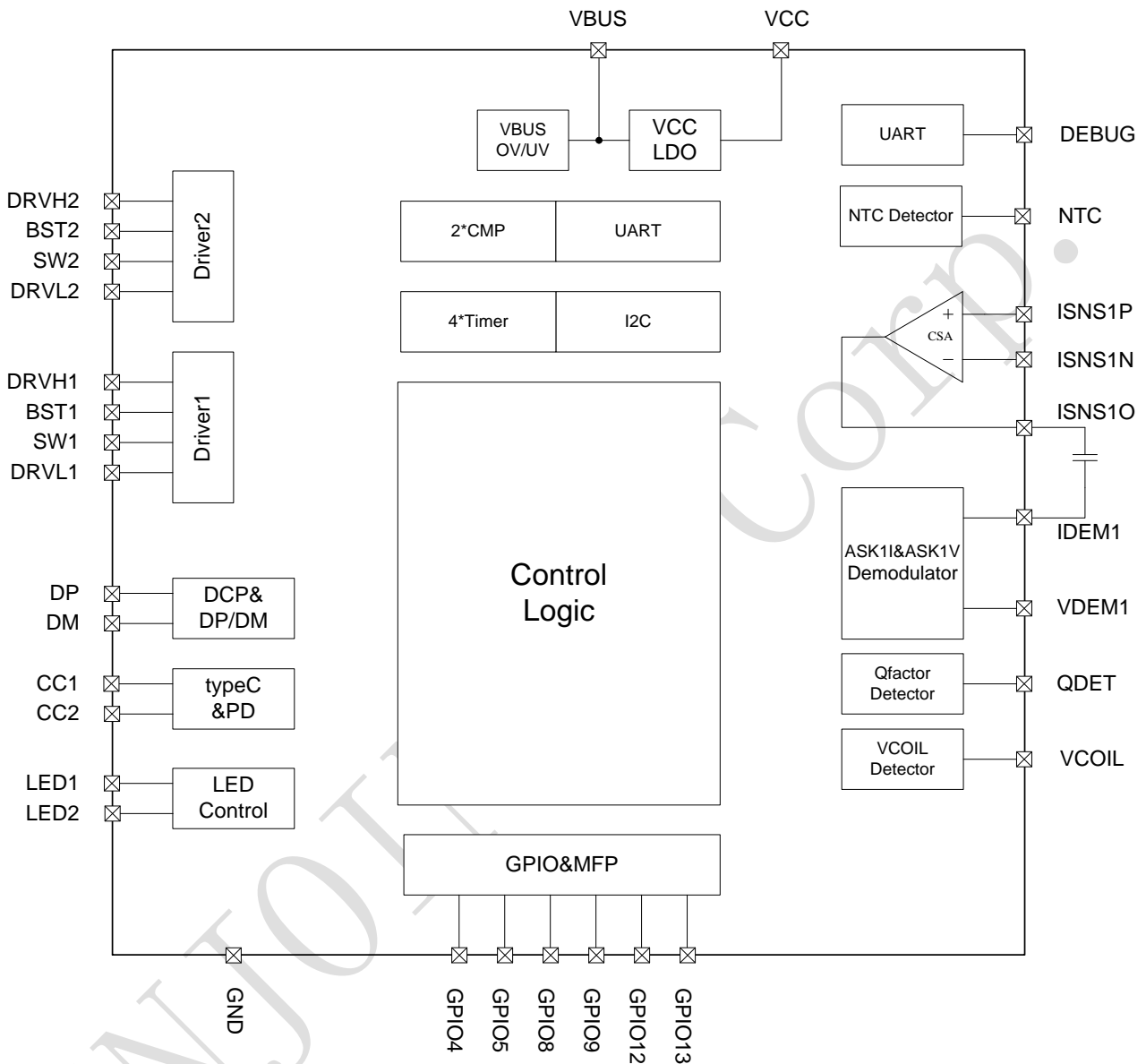


Figure 2 Functional Block Diagram

7 Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Voltage Range	V _{IN}	-0.3	26	V
	CC1, CC2	-0.3	12	
	DP, DM	-0.3	8	
Junction Temperature Range	T _J	-40	125	°C
Storage Temperature Range	T _{stg}	-60	125	°C
Package Thermal Resistance (Junction Temperature to environment)	θ _{JA}		40	°C/W
Human Body Model (HBM)	ESD		4	KV

* Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

8 Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Input Voltage Range	V _{IN}	4.0	5/9/12	21.5	V
I/O Voltage Range	IO4/5/8/9/12/13	GND-0.3		V _{CC} +0.3	V
	DP, DM, CC1, CC2	GND-0.3		5.5	
	LED1, LED2	GND-0.3		V _{CC} +0.3	
	NTC	GND-0.3		V _{CC} +0.3	

*Devices' performance cannot be guaranteed when working beyond those Recommended Operating Conditions.

9 Electrical Characteristics

Unless otherwise specified, T_A = 25°C

Parameters	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage	V _{IN}		4.0	5/9/12	21.5	V
Internal power supply	V _{CC}		3.0	3.6	5	V
Input high level	V _{IH}		0.7*V _{CC}			V
Input low level	V _{IL}				0.3*V _{CC}	V
Input high level	V _{OH}			V _{CC}		V
Input low level	V _{OL}			GND		V
LED Output current capability	Source current (LED1、LED2)	Source current to output high level is 0.8*V _{CC}		2	4	mA

10 Function Description

10.1 Fast Charge Input Request

Built-in PD protocol input request module, apply fast charging voltage to PD adapter through CC1, CC2.

Built-in DP&DM input fast charging protocol request module, apply fast charging voltage to the adapter through DP&DM.

10.2 Full Bridge Drive and Digital Demodulation

The IP6802 has a built-in 4N full-bridge driver, and the peripheral circuit needs to build a full-bridge 4xNMOS to implement the wireless charging controller.

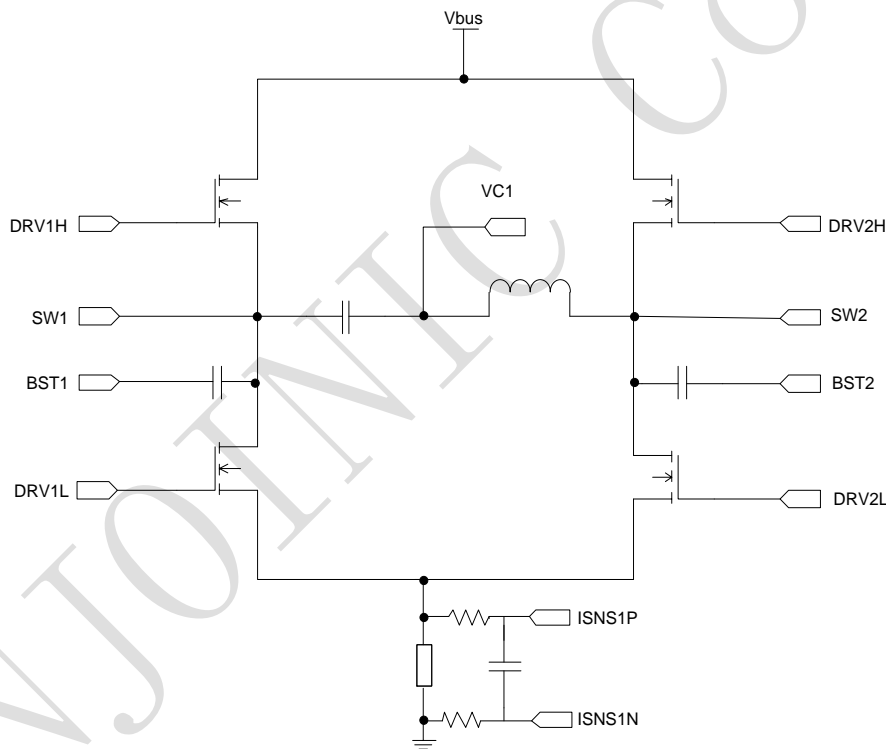


Figure 3 4xNMOS Full-Bridge Driver Application Circuit

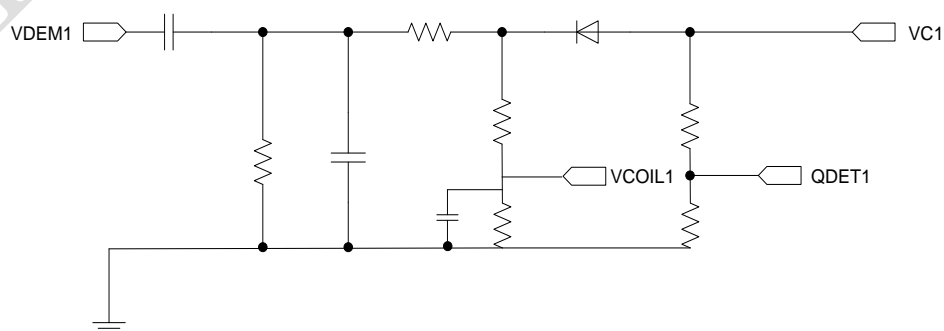


Figure 4 4xNMOS Voltage Decoder Circuit

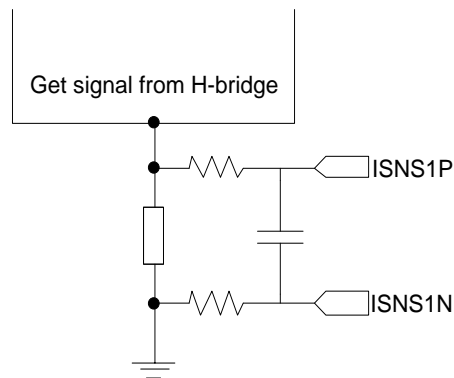


Figure 5 4xNMOS Current Decoder Circuit

10.3 DPM

For USB power supply with insufficient power supply capacity, it has dynamic power management function to keep the charging state uninterrupted. When the system detects that the input voltage is below 4.3V, the DPM function is activated to reduce the transmit power and hold it. When the input voltage returns to above 4.75V and the input current is reduced by 200mA compared to when it entered DPM, the system exits the DPM state.

10.4 FOD Parameter Adjustment

IP6802 supports static FOD foreign object detection and dynamic FOD foreign object detection.

Static FOD means that foreign objects on the coil can be detected when there is no wireless charging.

Dynamic FOD means being in the process of wireless charging and being able to detect foreign objects on the coil.

IP6802 can detect the Q value before entering charging to determine whether foreign objects exist, and can use the power loss method to determine whether foreign objects are present after entering charging.

10.5 NTC Thermal Protection

The NTC pin of IP6802 has a 20 μ A fixed output current, and the NTC PIN determines the NTC temperature by sampling the voltage of the NTC pin; this shutdown feature is to provide enhanced applications and is not limited to thermal shutdown. When the voltage of NTC pin is less than 0.5V, the system will enter NTC protection and end power transfer; after entering NTC protection, the NTC pin voltage is greater than 0.72V and normal charging resumes; if NTC application is not used, the pin is grounded through 100K resistor.

1.Refer to the NTC resistor data sheet to find the resistance - temperature relationship table

2.According to the protection temperature point, find the corresponding resistance value R_NTC

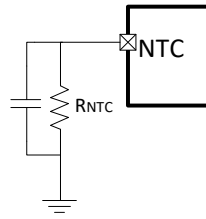


Figure 6 NTC Detection Circuit

Thermistor Recommended Parameters: $R_{NTC}=100K@25^{\circ}C$ $B=3950$;

10.6 Charging Indicator

IP6802 built-in indicator model algorithm, support user-defined charging indicator (need to use the PC upper computer provided by the original factory), import the firmware to the upper computer software, configure the indicator effect on the software interface, and export the new firmware to get the required indicator effect.

The default firmware LEDs correspond to each state light display as follows:

Charge Status	LED1	LED2
Power On	Blink 3 Times	Blink 3 Times
Standby	OFF	OFF
Charging	ON	OFF
FOD	OFF	Blink
Over Temperature	OFF	Blink
Overvoltage/Undervoltage	OFF	Blink
Charging Completed	OFF	ON

Each charging status light display can be flexibly configured or customized to achieve, such as charging breathing light, abnormal flashing and other charging indicators.

10.7 Efficiency Curve Test

Using IDT P9221 solution for RX device, the relationship of efficiency and system output power

$$\eta_{\text{system}} = \frac{P_{OL}}{P_{in}}$$

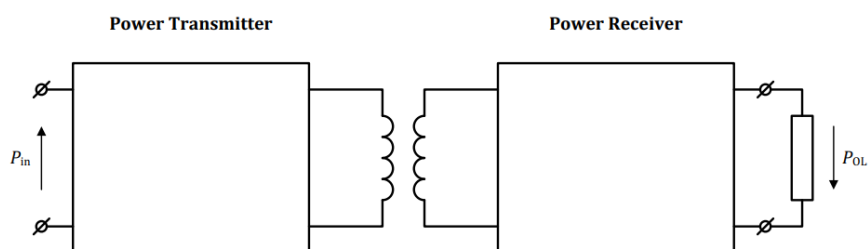


Figure 7 Wireless Charging Power Conversion Model

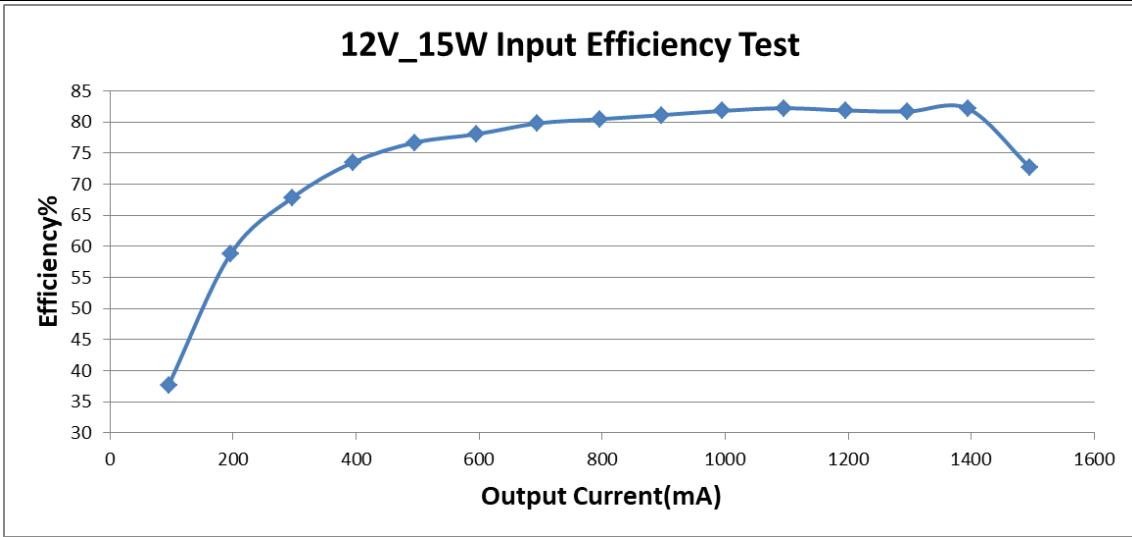


Figure 8 Loaded 15W Efficiency (Use IDT P9221_R RX)

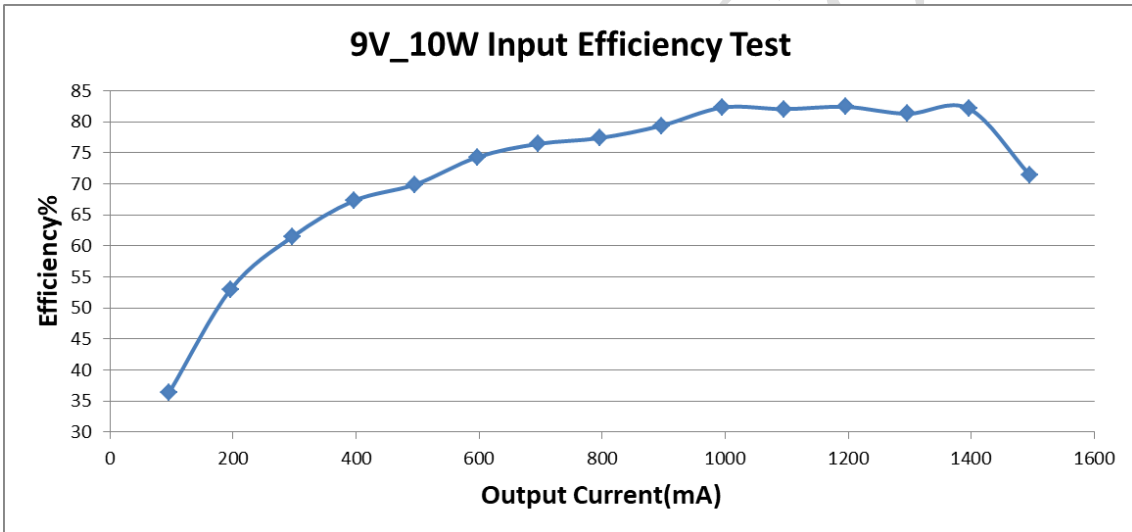


Figure 9 Loaded 10W Efficiency (Use IDT P9221_R RX)

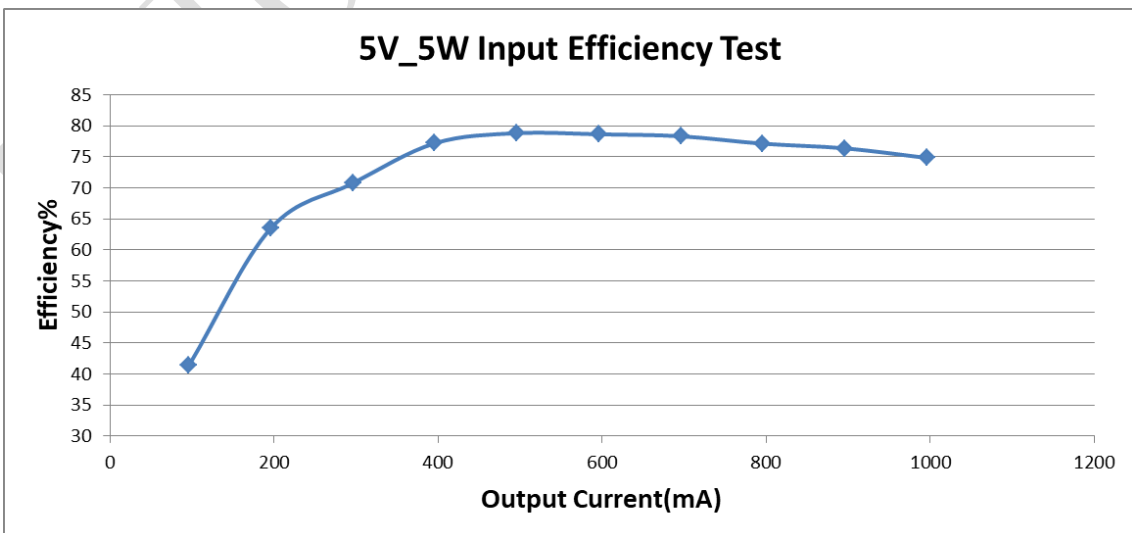


Figure 10 Loaded 5W Efficiency (Use IDT P9221_R RX)

11 Application Notes

IP6802 can be used with different transmitting coils and resonant capacitors to realize different power wireless charging solutions.

12 Firmware Upgrade Instructions

IP6802 integrates MTP ROM, supports multiple firmware upgrades, and the firmware download interface is DP/DM pins. The firmware download interface is DP/DM pin. To download the firmware, use the burner provided by the original manufacturer.

INJOINIC Corp.

13 Typical Application Schematic

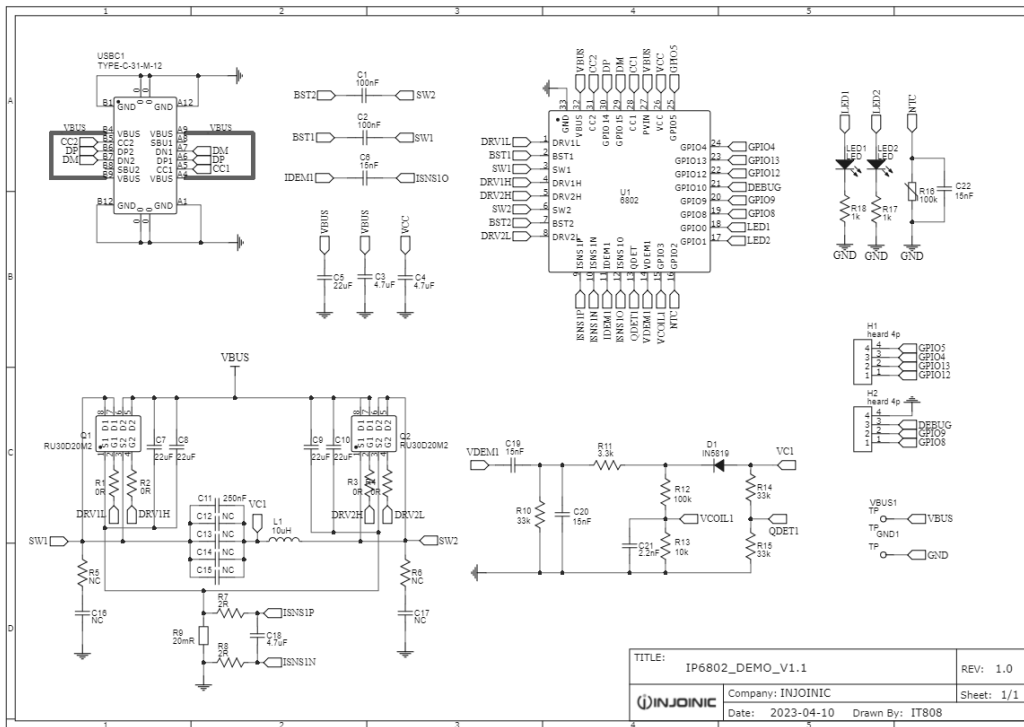


Figure 11 Typical Application Schematic

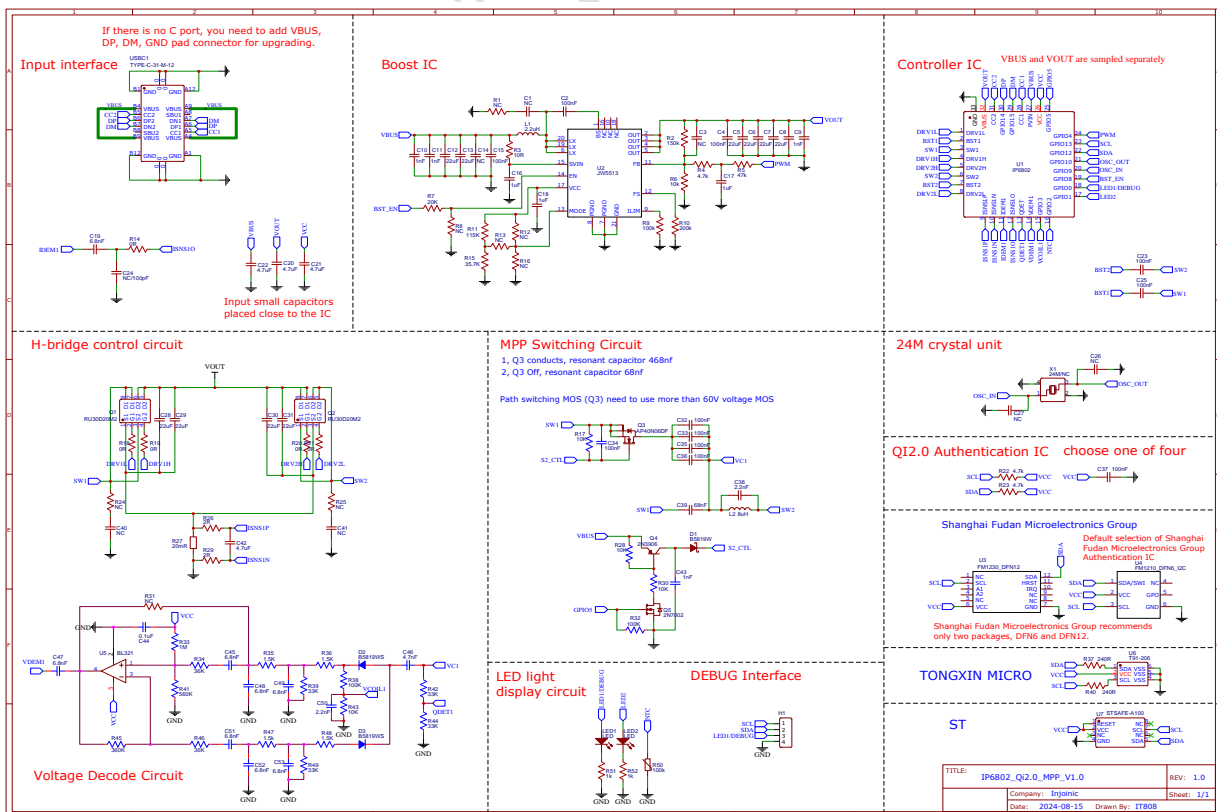
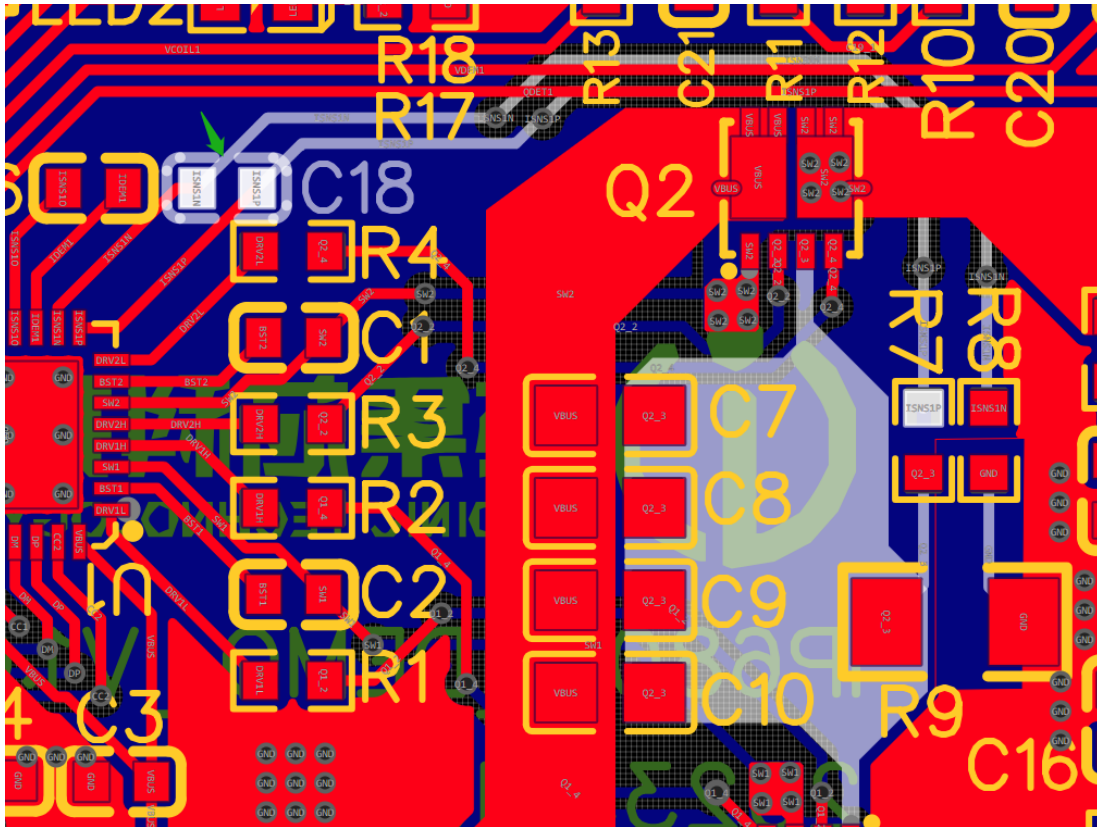


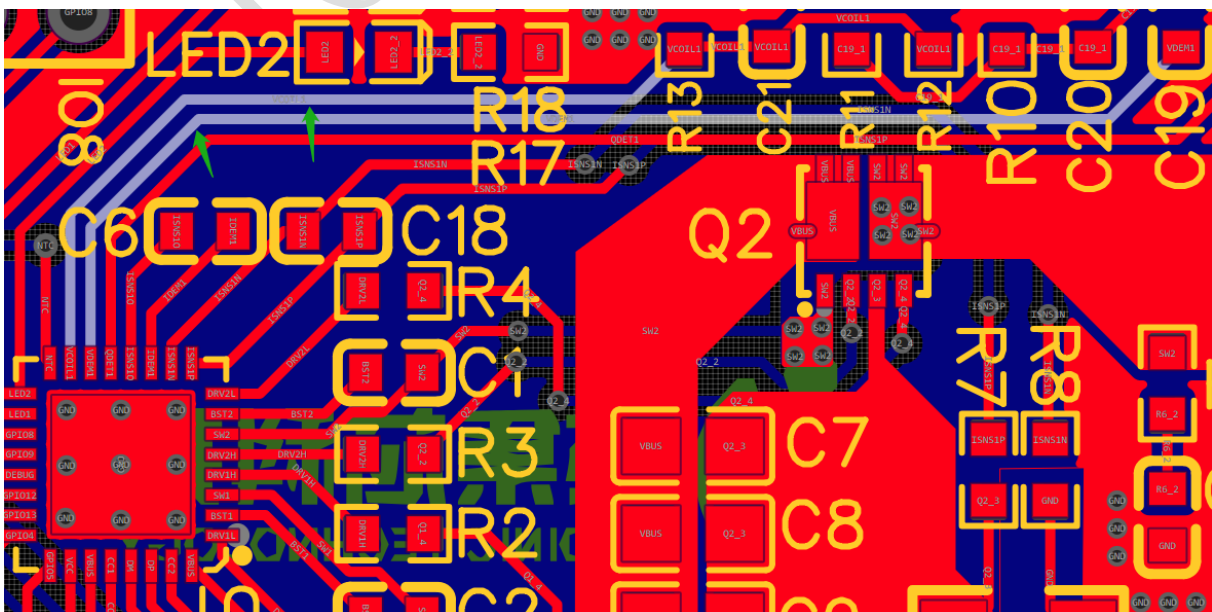
Figure 12 MPP Certification Schematic

14 Layout Notes

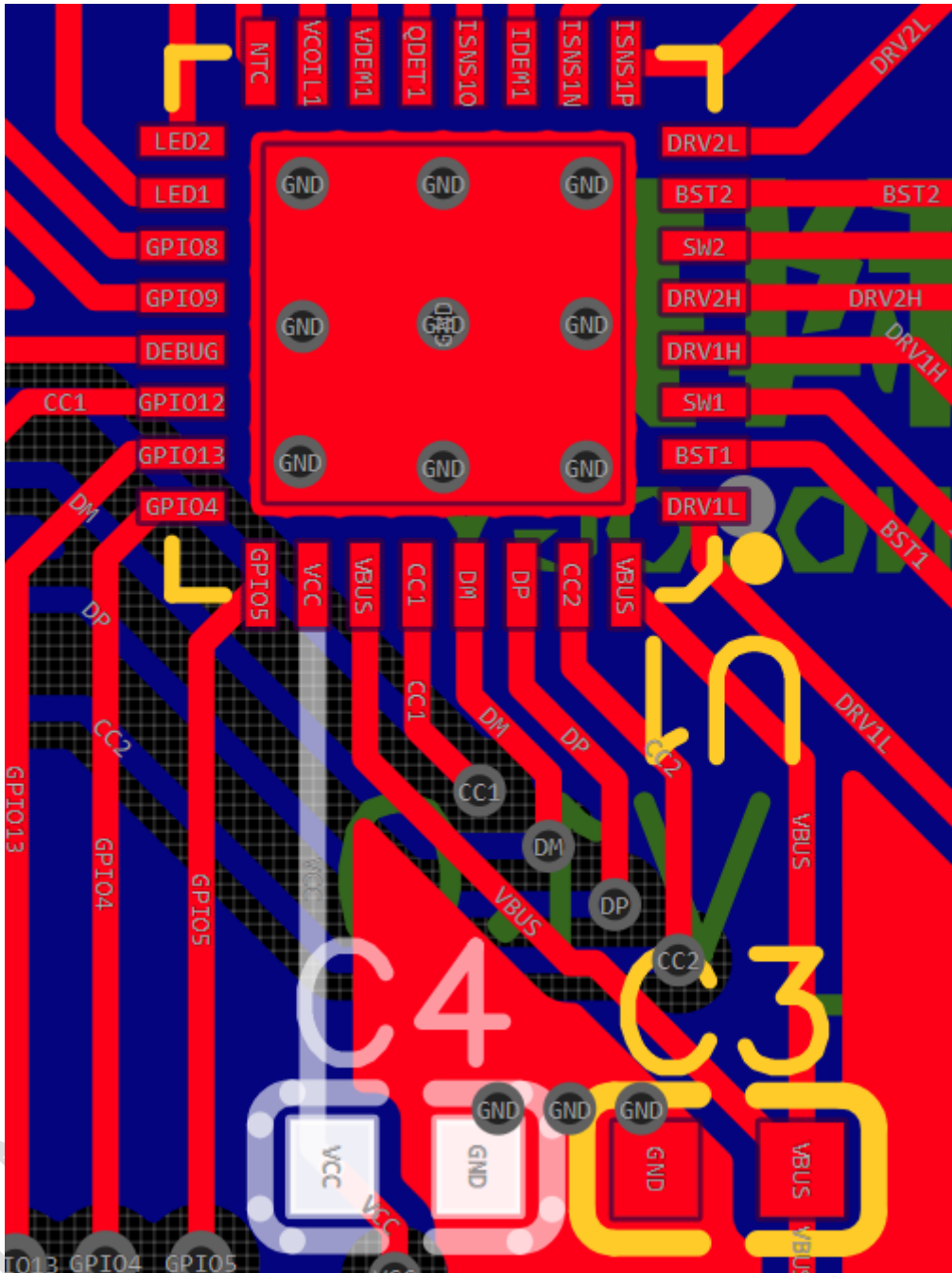
As shown in the figure below: the positive pole and negative pole of the 20mR Jepsun Sampling resistor need to be individually differential pair to the IC's ISNS1P and ISNS1N; and the routing of GND needs to be separated from the copper laying of GND, there can be no overlap.



As shown in the figure below: the VCOIL and VDEM of IP6802 should be wrapped with ground treatment, as far as possible from resonant capacitors, coils and other power lines; including the drive signal of IP6802, it is best to do wrapped ground treatment, away from resonant capacitors and coils.



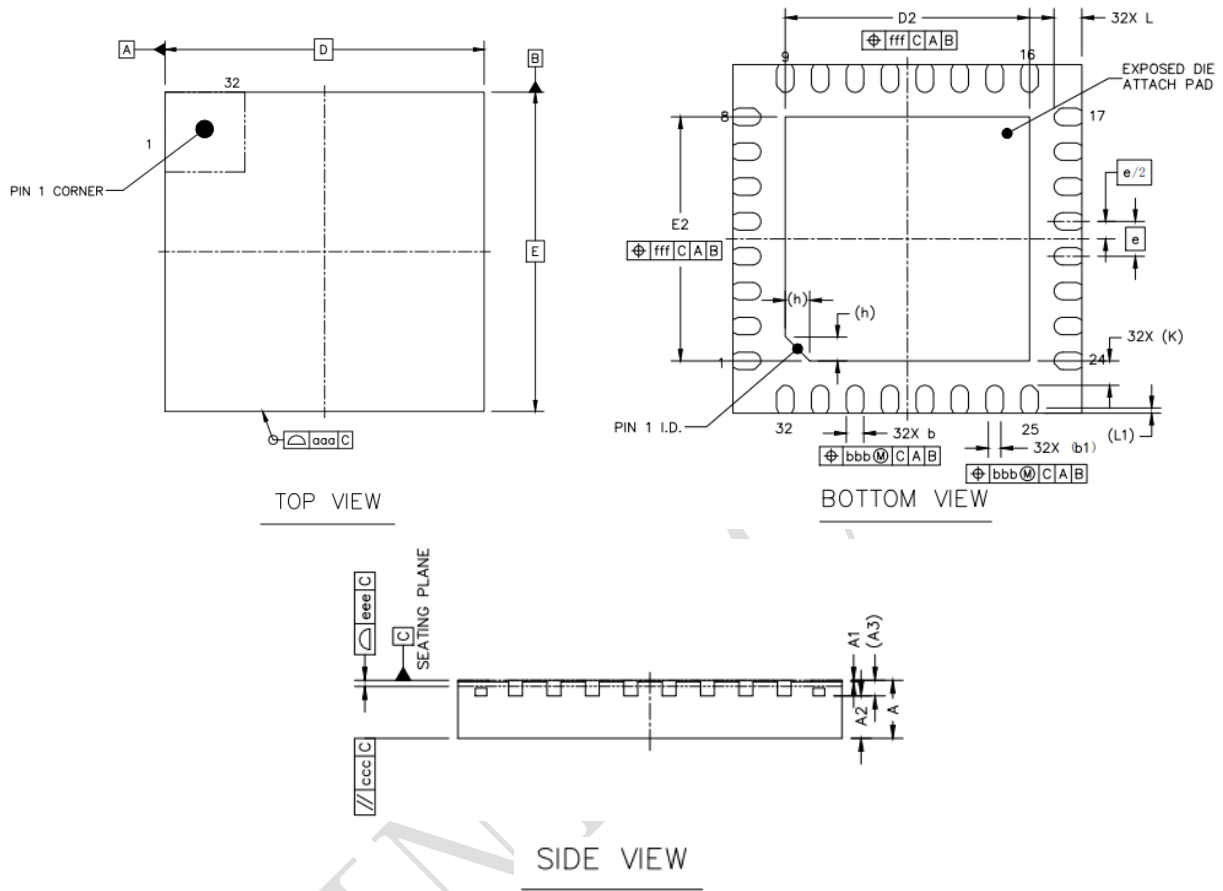
As shown in the figure below, the VCC capacitor of IP6802 needs to be placed close to the IC pin.



15 BOM

Item	Part Name	Description&Specification	Description	Qty	Note
1	100nF	C0603	C1, C2	2	
2	4. 7uF	C0603	C3, C4, C18	3	
3	22uF	C0805	C5, C7, C8, C9, C10	5	
4	15nF	C0603	C6, C19, C20, C22	4	
5	250nF	CBB	C11	1	
6	2. 2nF	C0603	C21	1	
7	IN5819	SOD-123F	D1	1	
8	10uH	MP_A2 线圈	L1	1	
9	LED	LED0603	LED1, LED2	2	
10	RU30D20M2	PDFN3333-8	Q1, Q2	2	
11	0R	R0603	R1, R2, R3, R4	4	
12	2R	R0603	R7, R8	2	
13	20mR	R1206_1	R9	1	
14	33k	R0603	R10, R14, R15	3	
15	3. 3k	R0603	R11	1	
16	100k	R0603	R12	1	
17	100k	R0603 100K@25°C B=3950	R16	1	
18	10k	R0603	R13	1	
19	1k	R0603	R17, R18	2	
20	TYPE-C-31-M-12	USB-C_SMD	USBC1	1	

16 Package



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.02	0.05
MOLD THICKNESS	A2	---	0.55	---
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.2	0.25	0.3
	b1	0.18 REF		
Epad Chamfer Dimension	h	0.35 REF		
BODY SIZE	X	D		
	Y	E		
LEAD PITCH	e	0.5 BSC		
EP SIZE	D2	3.4	3.5	3.6
	E2	3.4	3.5	3.6
LEAD LENGTH	L	0.35	0.4	0.45
	L1	0.075 REF		
LEAD TIP TO EXPOSED PAD EDGE	K	0.35 REF		
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	ccc	0.1		
COPLANARITY	eee	0.08		
LEAD OFFSET	bbb	0.1		
EXPOSED PAD OFFSET	fff	0.1		

17 Silk Information



18 IMPORTANT NOTICE

INJOINIC TECHNOLOGY and its subsidiaries reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to INJOINIC TECHNOLOGY's terms and conditions of sale supplied at the time of order acknowledgment.

INJOINIC TECHNOLOGY assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using INJOINIC TECHNOLOGY's components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of INJOINIC TECHNOLOGY's components in its applications, notwithstanding any applications-related information or support that may be provided by INJOINIC TECHNOLOGY. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify INJOINIC TECHNOLOGY and its representatives against any damages arising out of the use of any INJOINIC TECHNOLOGY's components in safety-critical applications.

Reproduction of significant portions of INJOINIC TECHNOLOGY's information in INJOINIC TECHNOLOGY's data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. INJOINIC TECHNOLOGY is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

INJOINIC TECHNOLOGY will update this document from time to time. The actual parameters of the product may vary due to different models or other items. This document voids all express and any implied warranties.

Resale of INJOINIC TECHNOLOGY's components or services with statements different from or beyond the parameters stated by INJOINIC TECHNOLOGY for that component or service voids all express and any implied warranties for the associated INJOINIC TECHNOLOGY's component or service and is an unfair and deceptive business practice. INJOINIC TECHNOLOGY is not responsible or liable for any such statements.